Docket No.: P2001,0216

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ANNALISA CAPPELLANI ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD FOR FABRICATING A MOSFET HAVING A VERY SMALL CHANNEL LENGTH

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 6,091,120 (Yeom et al.), dated July 18, 2000;

U.S. Patent No. 5,089,863 (Satoh et al.), dated February 18, 1992;

U.S. Patent No. 5,384,479 (Taniguchi), dated January 24, 1995, and corresponding German Patent DE 42 34 528 C2 (Taniguchi), dated April, 15, 1993;

German Published Non-Prosecuted Patent Application DE 42 34 777 A1 (König et al.), dated April 21, 1994, and English abstract thereof;

French Patent Application FR 2 791 177 A1 (Thomas et al.), dated September 22, 2000, and English abstract thereof;

Patent Abstracts of Japan 63044768 (Shinichi), dated February 25, 1988;

European Patent Application EP 0 740 334 A2 (Eckstein et al.), dated October 30, 1996;

European Patent Application EP 0 328 350 A2 (Nakamura et al.), dated August 16, 1989;

PCT WO 02/41383 A1 (Furukawa et al.), dated May 23, 2002;

Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2nd Edition, pp. 201-203;

Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418;

Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $TiSi_2$ and $CoSi_2$ ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269;

Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1-μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956;

Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500;

International Search Report, dated April 14, 2003.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicants

Date: September 26, 2003

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/nt/kf

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.: P2001,0216
Appl. No.:

Applicant: ANNALISA CAPPELLANI ET AL.

Filing Date: September 26, 2003
Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	6,091,120	7/18/00	Yeom et al.			
	B	5,089,863	2/18/92	Satoh et al.			
	C	5,384,479	1/24/95	Taniguchi			
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	42 34 528 C2	4/15/93	Germany				
	K	42 34 777 A1	4/21/94	Germany				
	L	2 791 177 A1	9/22/00	France				
	M	63044768	2/25/88	Japan				
	N	0 740 334 A2	10/30/96	Europe				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2nd Edition, pp. 201-203
		Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418

EXAMINER	DATE CONSIDERED

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: P2001,0216 Appl. No.: Applicant: ANNALISA CAPPELLANI ET AL. Filing Date: September 26, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	0 328 350 A2	8/16/89	Europe				
	K	02/41383 A1	5/23/02	WIPO				
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $TiSi_2$ and $CoSi_2$", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269
		Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1-μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956

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		Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500

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